REMARKS

This Amendment is in response to the Office Action dated September 9, 2002. Claims 10-21 are pending. Claims 10-21 are rejected. Claims 10 and 16 have been amended. Accordingly, claims 10-21 remain pending in the present application.

Applicant includes a Petition for Extension of Time to extend the deadline for filing a response by two (2) months from December 9, 2002 to February 9, 2003.

Drawings

Examiner states,

In figure 5, there is no the edge marked 506.

Figure 5 has been corrected in accordance with the Examiner's instructions to mark the edge 506.

Specification

Examiner states,

Page 1, submit two applications entitled "Buried Power buss for High Current, High Power semiconductor Devices..., serial no. 2198P, 2208P.

The cross-reference information requested by Examiner, consisting of serial numbers and filing dates for both of the above-referenced applications has been added to the paragraph on page 1, beginning at line 2, in accordance with Examiner's instructions.

Examiner states,

Also, page 19, line 16, "lower int4erconnect sheet" should be – lower interconnect sheet—

In the paragraph on page 19, line15, the correction has been made in accordance with Examiner's instructions.

Claim Rejections – 35 USC § 102(b)

Examiner states,

Claims 10-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada (6,008,127).

Regarding claim 10, Yamada, figures 1-38, (figures 33, 35, 36, 37, col. 8, lines 52-67), lines 1-67), disclose a semiconductor device comprising: a semiconductor substrate 201 including a plurality of device structures (see figure 35) thereon; and an interconnect 235 on the semiconductor substrate, the interconnect comprising at least one slot 235 (see figure 33) provided in the semiconductor substrate and at least one metal 235 (aluminum) within the slot, wherein the at least one slot is oxidized everywhere (see col. 8, lines 52-67) except at the bottom of the slot where the interconnect forms a ground 225 (see col. 9, lines 58-65). Regarding to claims 11-15, see Yamada, col. 1-14, lines 1-67.

Applicant traverses this rejection. Applicant has amended claim 10 to clarify the present invention. The present invention as recited in claim 10 provides for a high voltage semiconductor device which includes a semiconductor substrate and an interconnect. The interconnect includes a slot in the substrate and at least one metal within the slot. The metal is of sufficient thickness to carry a high current. The Yamada ('127) neither teaches nor suggests such a device.

Yamada is directed to a process for fabricating a semiconductor device using an etching stopper film which does not increase the number of photo-etching steps and does not cause a deterioration in device characteristics. It is directed to a conventional semiconductor device and is not concerned with and is not directed toward a high voltage or high power semiconductor device. Furthermore, there is no teaching or suggestion that the metal within the contact holes of Yamada are of sufficient thickness to carry a high current as recited in claim 10. Accordingly, claim 10 is allowable over the cited reference. Furthermore, claims 11-15 are also allowable and they depend from an allowable base claim.

Claim Rejections 35 USC § 102(b)

Examiner states,

Claims 16-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada (6,008,127).

Regarding claim 16, Yamada, figures 1-38, (figures 33, 35, 36, 37, col. 8, lines 52-67, col. 9, lines 1-67), disclose a high voltage interconnect on a semiconductor device comprising: at least one slot 235 provided in the semiconductor substrate 201; and at least one metal 235 (aluminum) within the slot, wherein the at least one slot is oxidized (col. 8, lines 52-67) everywhere except at the bottom of the slot, and the interconnect forms a very low resistance ground trap 225 (see col. 5, lines 61-67, col. 9, lines 15-22, lines 58-65).

Regarding claims 17-21, see Yamada, col. 1-14, lines 1-67.

Applicant traverses this rejection. Applicant has amended claim 16 to clarify the present invention. The present invention as recited in claim 16 provides for a high voltage on a semiconductor substrate. The interconnect includes a slot in the substrate and at least one metal within the slot. The metal is of sufficient thickness to carry a high current. The Yamada ('127) neither teaches nor suggests such a device.

Yamada is directed to a process for fabricating a semiconductor device using an etching stopper film which does not increase the number of photo-etching steps and does not cause a deterioration in device characteristics. It is directed to a conventional semiconductor device and is not concerned with and is not directed toward a high voltage interconnect. Furthermore, there is no teaching or suggestion that the metal within the contact holes of Yamada are of sufficient thickness to carry a high current as recited in claim 16. Accordingly, claim 16 is allowable over the cited reference. Furthermore, claims 17-21 are allowable since they depend from an allowable base claim.

Conclusion

Therefore, for the above identified reasons, the present invention as recited in independent claims 10 and 16 is neither taught nor suggested by the cited references. Applicant

further submits that claims 11-15 and 17-21 are also allowable because they depend on the above allowable base claims.

In view of the foregoing, Applicant submits that claims 10-21 are patentable over the cited reference. Applicant, therefore, respectfully requests reconsideration and allowance of the claims as now presented.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made"**.

Applicants' attorney believes this application in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted,

Joseph A. Sawyer, Jr.
Sawyer Law Group LLP
Attorney for Applicant
Reg. No. 30,801
(650) 493-4540

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE DRAWINGS

Figure 5 has been corrected in accordance with Examiner's recommendations to mark the edge 506.

IN THE SPECIFICATION

Please replace the paragraph beginning at page 1, line 2, with the following rewritten paragraph:

The present application is related to the following listed two applications: Serial No. [✓] 10/034,184 (filed 12/28/2001) [(2193P)], entitled "Buried Power Buss for High Current, High Power Semiconductor Devices and A Method for Providing the Same;" and Serial No. [✓] 10,034067 (filed 12/28/2001) [(2208P)], entitled "Buried Power Buss Utilized as A Sinker for High Current, High Power Semiconductor Devices and A Method for Providing the Same"; assigned to the assignee of the present application, and filed on the same date.

Please replace the paragraph beginning at page 19, line 15, with the following rewritten paragraph:

A method and system for providing an interconnect on a semiconductor device is disclosed. This method, called the buried power buss results in lower int[4]erconnect sheet resistance versus standard approaches. The method provides additional capability since it results in oxide isolation in place of junction isolation and allows the long junction isolation process to be eliminated. Oxide isolation results in lower leakage and capacitance than the standard junction isolation. This approach results in the metal having an oxide jacket thus allowing metal to be connected while isolating itself from other circuit functions. The method provides a

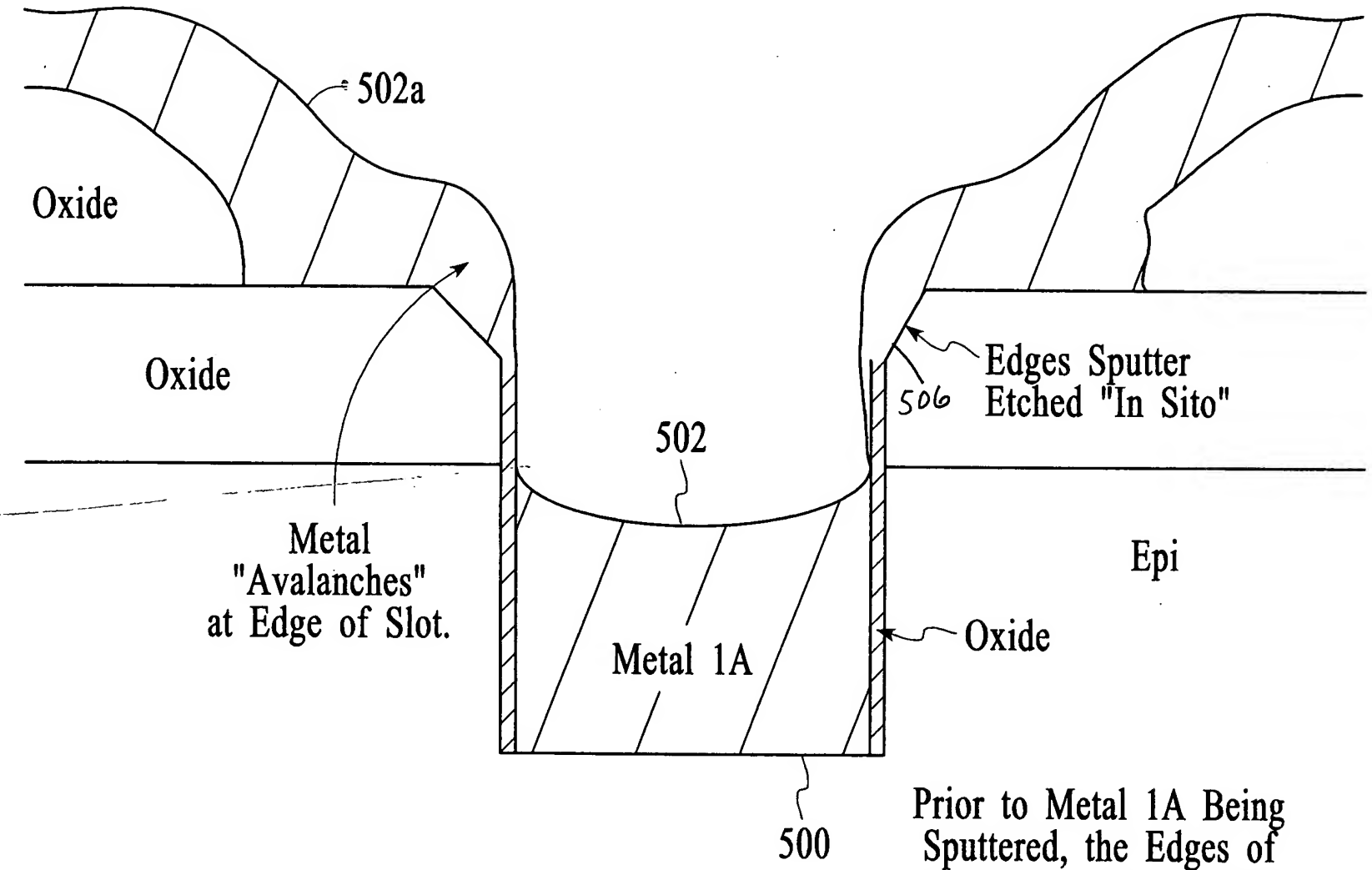

FIG. 5